Amendments to Claims

Listing of Claims:

1. (Currently amended) An apparatus comprising:

an electrically powered physical layer interface to interface between a PCI-type bus and a network, the physical layer interface having a high power state, a first low power state, and a second low power state; and

a power management system configured to transition the physical layer interface from the high power state to one of the low power states when a PCI reset signal assertion ~~signal~~ is detected on the PCI-type bus.

2. (Currently amended) The apparatus of claim 1, wherein the PCI-type bus is a PCI bus.

3. (Currently amended) The apparatus of claim 1, wherein the PCI-type bus is a PCI-X bus.

4-5. (Cancelled)

6. (Previously Presented) The apparatus of claim 1, wherein the first low power state is when the physical layer interface is powered off.

7. (Previously Presented) The apparatus of claim 6, wherein the second low power state is a state in which the physical layer interface draws no more than a predetermined amount of current.

8-9. (Cancelled)

10. (Currently amended) ~~The apparatus of claim 1~~ An apparatus comprising:

an electrically powered physical layer interface to interface between a bus and a network, the physical layer interface having a high power state, a first low power state, and a second low power state; and

a power management system configured to transition the physical layer interface from the high power state to one of the low power states when a signal is detected on the bus, wherein the power management system is incorporated within a Gigabit Ethernet device.

11. (Previously Presented) The apparatus of claim 10, wherein the first low power state is a state in which the physical layer interface is transmitting or receiving data at no greater than 100 megabits per second.

12. (Currently amended) A system comprising:

a power supply;

a PCI-type bus electrically connected to the power supply;

a central processing unit in communication with the PCI-type bus; and

a communications device in communication with PCI-type bus, the communications device comprising:

an electrically powered physical layer interface having a high power state, a first low power state, and a second low power state; and

a power management system configured to transition the physical layer interface to the low power state when a PCI reset signal assertion ~~signal~~ is detected on the PCI-type bus.

13. (Currently amended) The system of claim 12, wherein the PCI-type bus is a PCI bus ~~and the signal is a PCI reset signal assertion~~.

14. (Currently amended) The system of claim 12, wherein the PCI-type bus is a PCI-X bus ~~and the signal is a PCI reset signal assertion~~.

15. (Cancelled)

16. (Previously Presented) ~~The system of claim 12,~~ A system comprising:

a power supply;

a bus electrically connected to the power supply;

a central processing unit in communication with the bus; and

a communications device in communication with bus, the communications device comprising:

an electrically powered physical layer interface having a high power state, a first low power state, and a second low power state, wherein the first low power state is an off state and the second low power state is a state in which the communications device transmits data at a reduced rate; and

a power management system configured to transition the physical layer interface to the low power state when a signal is detected on the bus.

17. (Currently amended) The system of claim 16, wherein the communications device includes a register having at least a one-bit field, and the system further comprises:

a storage device;

an operating system stored on the storage device and configured to write data to the field in the register if wake up of the communications device is enabled or disabled; and

wherein the power management system is configured to transition the first or second power state depending upon ~~wheather~~ whether wake up is enabled or disabled.

18. (Currently amended) The system of claim 16~~12~~, wherein the communications device is a Gigabit Ethernet device.

19. (Previously Presented) The system of claim 18, wherein one of the low power state of the physical layer interface is a state in which the physical layer interface transmits or receives data at less than or equal to 100 megabits per second.

20. (Original) The system of claim 12, wherein the communication device is a wireless local area network controller.

21. (Previously Presented) The system of claim 18 wherein the power management system is incorporated within the Gigabit Ethernet device.

22. (Currently amended) A method comprising:

within a networked computer system having an operating system, monitoring a bus that supplies power to a Gigabit Ethernet device that includes a register and an electrically powered physical layer interface, wherein the physical layer interface is configured to include a high power state, a first low power state in which the physical layer interface is not enabled to transmit data to or receive data from the network, and a second low power state;

writing data to the register by the operating system to indicate whether wake up of the device is enabled or disabled; and

changing the power state of a physical layer interface to the first or second low power state when a signal is detected on the bus depending upon whether wake up of the device has been enabled.

23-26. (Cancelled)

27. (Currently amended) The method of claim 22 ~~26~~ wherein the second low power state is a state in which the physical layer interface is configured to transmit data to or receive data from the network at rates up to 100 megabits per second.

28. (Previously Presented) The method of claim 27 wherein the bus is a PCI-type bus.

29. (Previously Presented) The method of claim 28 wherein the signal is a PCI reset assertion.

30. (Currently amended) A computer program product residing on a computer readable medium for powering down a physical layer interface, comprising instructions for causing an instruction processor to:

monitor a bus for assertion of a signal on the bus; and

reduce the power state of the physical layer interface from a high power state to either a first or second low power state when the signal is detected on the bus;

write data to a register by the operating system to indicate whether wake up of the device is enabled or disabled; and

reduce the power state of the physical layer interface to the first low power state if the data in the register indicates that wake up is disabled at the time the signal is detected or to the second low power state if the data in the register indicates that wake up is enabled at the time the signal is detected.

31. (Original) The computer program product of claim 30 wherein the device is a Gigabit Ethernet device.

32. (Cancelled)